8-Bit High-Speed Multiplying D/A Converter

DAC08

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at http://www.analog.com/aerospace is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/DAC08

2.0 Part Number. The complete part number(s) of this specification follow:

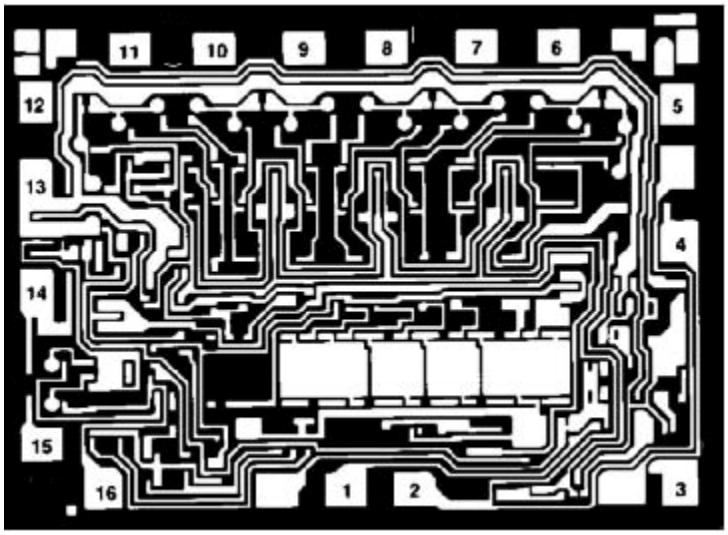
Part Number	Description
DAC08-000C	8-Bit High-Speed Multiplying D/A Converter
DAC08R000C	Radiation guaranteed 8-Bit High-Speed Multiplying D/A Converter

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness	Bond Pad Metalization
63 mil x 87 mil	19 mil ± 2 mil	Al/Cu

3.2 Die Picture



1. V_{LC}
2. $\overline{I_{OUT}}$
3. V-
4. I_{OUT}
5. B1 (MSB)
6. B2
7. B3
8. B4
9. B5
10. B6
11. B7
12. B8 (LSB)
13. V+
14. V_{REF+}
15. V_{REF-}
16. COMP

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3.3 Absolute Maximum Ratings 1/

Supply Voltage (V+ to V-)	36V dc
Logic Inputs	V- to (V- plus 36V dc)
Logic Control Voltage (V_{LC})	V- to V+
Analog Current Outputs (at V- = 15V)	4.25mA
Reference Input (V_{REF+} to V_{REF-})	V- to V+
Reference Input Differential Voltage (V_{REF+} to V_{REF-})	±18V dc
Reference Input current (I_{VREF+})	5mA
Storage Temperature Range	-65°C to +125°C
Ambient Operating Temperature Range (T_A)	-55°C to +125°C
Junction Temperature (T_J)	+150°C

Absolute Maximum Ratings Notes:

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.

(a) Qual Sample Size and Qual Acceptance Criteria – 25/2

(b) Qual Sample Package – DIP

(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I - Dice Electrical Characteristics					
Parameter	**Symbol**	**Conditions 1/**	**Limit Min**	**Limit Max**	**Units**
Power Supply	I+	$V_S = \pm15V$; $I_{REF} \leq 2mA$		3.8	mA
	I-		-7.8		
Full Range Current	I_{FR}	$V_{REF} = 10V$, $R_{14}, R_{15} = 5k\Omega$	1.94	2.04	mA
Output Voltage Compliance	V_{OC}	Full Range Current Change < 1/2 LSB	-10	18	V
Zero Scale Current	I_{ZS}			2	µA
Full Range Symmetry	I_{FRS}	$I_{FR} - \overline{I_{FR}}$		±8	µA
Output Current Range	I_{OR1}	$V_{REF} = 15V$, V- = -10V, $R_{14}, R_{15} = 5k\Omega$	2.1		mA
	I_{OR2}	$V_{REF} = 25V$, V- = -12V, $R_{14}, R_{15} = 5k\Omega$	4.2		
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5V to 18V, V- = -18V; $I_{REF} = 1mA$		±0.01	$\frac{\%\Delta I_O}{\%\Delta V+}$
	$PSSI_{FS-}$	V- = -4.5V to -18V, V+ = +18V; $I_{REF} = 1mA$		±0.01	$\frac{\%\Delta I_O}{\%\Delta V-}$
Reference Bias Current	I_{VREF-}		0	-3	µA
Logic Input Levels	V_{IL}	Logic "0", $V_{LC} = 0V$		0.8	V
	V_{IH}	Logic "1", $V_{LC} = 0V$	2		
Logic Input Current (Each Bit)	I_{IL}	$V_{IN} = -10V$, $V_{LC} = 0V$		-10	µA
	I_{IH}	$V_{IN} = 18V$, $V_{LC} = 0V$		+10	
Logic Input Swing	V_{IS}	$I_{FR} = 1.94mA$ (min) $I_{FR} = 2.04mA$ (max)	-10	+18	V
Resolution			8		Bits
Monotonicity			8		Bits
Nonlinearity	NL			±0.1	%FS

Table I Notes:

1. $V_S = \pm15V$, $I_{REF} = 2mA$, and $T_A = +25°C$, unless otherwise specified.

Table II - Electrical Characteristics for Qualification						
Parameter	**Symbol**	**Conditions 1/**	**Sub-groups**	**Limit Min**	**Limit Max**	**Units**
Power Supply 2/	I+	$V_S = \pm15V$ or +5V, -15V	1, 2, 3		3.8	mA
		$V_S = \pm5V$, $I_{REF} = 1mA$				
		M, D, L, R			4.0	
	I-	$V_S = \pm15V$ or +5V, -15V	1, 2, 3	-7.8		
		$V_S = \pm5V$; $I_{REF} = 1mA$	1, 2, 3	-5.8		
		M, D, L, R 3/	1	-8.0		
Full Range Current	I_{FR}	$V_{REF} = 10V$, R_{14}, $R_{15} = 5k\Omega$	1, 2, 3	1.94	2.04	mA
		M, D, L, R 3/	1	1.925	2.04	
Output Voltage Compliance 4/	V_{OC}	Full-Scale Current Change < 1/2 LSB	1, 2, 3	-10	+18	V
Zero Scale Current	I_{ZS}		1, 2, 3		2	µA
		M, D, L, R 3/	1		2	
Full Range Symmetry 4/	I_{FRS}	$I_{FR} - \overline{I_{FR}}$	1, 2, 3		±8	µA
Output Current Range 4/	I_{OR1}	$V_{REF} = 15V$, V- = -10V; R_{14}, $R_{15} = 5k\Omega$	1, 2, 3	2.1		mA
	I_{OR2}	$V_{REF} = 25V$, V- = -12V; R_{14}, $R_{15} = 5k\Omega$		4.2		
Power Supply Sensitivity 4/	$PSSI_{FS+}$	V+ = 4.5V to 18V, V- = -18V, $I_{REF} = 1mA$	1, 2, 3		±0.01	$\frac{\%\Delta I_O}{\%\Delta V+}$
	$PSSI_{FS-}$	V- = -4.5V to -18V, V+ = 18V, $I_{REF} = 1mA$			±0.01	$\frac{\%\Delta I_O}{\%\Delta V-}$
Reference Bias Current 4/	I_{VREF-}		1, 2, 3	0	-3	µA
Logic Input Levels	V_{IL}	Logic "0", $V_{LC} = 0V$	1, 2, 3		0.8	V
		M, D, L, R 3/	1		0.8	
	V_{IH}	Logic "1", $V_{LC} = 0V$	1, 2, 3	2.0		
		M, D, L, R 3/	1	2.0		
Logic Input Current (Each Bit) 4/	I_{IL}	$V_{IN} = -10V$, $V_{LC} = 0V$	1, 2, 3		-10	µA
		M, D, L, R 3/	1		-30	
	I_{IH}	$V_{IN} = 18V$, $V_{LC} = 0V$	1, 2, 3		10	
		M, D, L, R 3/	1		10	
Logic Input Swing 4/	V_{IS}	$I_{FR} = 1.94mA$ (min) $I_{FR} = 2.04mA$ (max)	1, 2, 3	-10	+18	V
Monotonicity 4/			1, 2, 3	8		Bits
Nonlinearity	NL		1, 2, 3		±0.19	%FS
		M, D, L, R 3/	1		±0.45	
Full Scale Tempco 4/	TCI_{FS}		8		±80	ppm/°C

Table II Notes:

1. $V_S = \pm15V$, $I_{REF} = 2mA$, unless otherwise specified.
2. When the device is used in an un-biased state at high temperature only, and subsequently biased, the device supply currents may rise 30% above specification for as long as 30 seconds.
3. Devices tested at 100K.
4. This parameter not tested post irradiation.

Table III - Life Test Endpoint and Delta Parameter (Product is tested in accordance with Table II with the following exceptions)								
Parameter	**Symbol**	**Sub-groups**	**Post Burn In Limit**		**Post Life Test Limit**		**Life Test Delta**	**Units**
			Min	**Max**	**Min**	**Max**		
`Full Range Current	I_{FR} $\overline{I_{FR}}$	1	1.93	2.05	1.92	2.06	0.01	mA
Zero Scale Current	I_{ZS} $\overline{I_{ZS}}$	1		2.5		3	0.5	μA

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	20-DEC-01
B	Update web address	Aug. 5, 2003
C	Add radiation limits same as SMD	Aug. 25, 2003
D	Update header/footer & add to 1.0 Scope description.	March 3, 2008
E	Add Junction Temperature (T_J) ....+150°C to Absolute Max. Ratings	April 2, 2008
F	Updated Section 4.0c note to indicated pre-screen temp testing being performed.	June 6 2009
G	Update fonts and sizes to ADI standards	Nov. 15, 2011